Lesson Planning for the semester started w.e.f. 5th Jan 2019

Name of Institute :- Sat Kabir Institute of Technology and Management, Ladrawan (Jhajjar)

Name of teacher with designation :- SUMIT DALAL, A.P.

Department :- ECE

Month	Class	Topic/Chapter Covered	Academic Activity	Test/Assignment
JAN	ECE-4th Sem	Comm. Systems: Introduction to Communication systems (1-2 week)	Ppt.	Assignment in 3rd week
		Basic concept of Modulation, Demodulators, MUX & DEMUX. (3-4 week)	Section revision	Test in 4th week.
JAN.	ECE-6th Sem	VLSI Design: Basic MOS transistor - Emode & De- mode. (2 week)	Ppt	Assignment in 3rd week
		Second order effect - MOS transistor Model. (2 week)	Section revision	Test in 4th week
JAN	MTech 2nd Sem	VLSI design: Review of MOS technology. (2 week)	Ppt	Assignment in 3rd week
		N-MOS, CMOS process, Production of masks. (2 week)	Section revision	Test in 4th week
FEB	ECE-4th Sem	Comm. Systems: Amplitude Modulation - Generation, demodulation, VSB (2 week)	Ppt	Assignment in 3rd week
		Angle Modulation - PM, FM, NBFM, WBFM. (2week)	Section revision	Test in 4th week
FEB	ECE-6th Sem	VLSI Design: N-MOS & CMOS Inverter & gates. (2week)	Ppt	Assignment in 3rd week
		Stick diagram - Lambda based design rules (2week)	Section revision	Test in 4th week
FEB	MTech 2nd Sem	VLSI Design: Electrical properties of MOS circuit (2week)	Ppt	Assignment in 3rd week
		MOS Transistor Model, Pull-up to pull-down ratio. (2week)	Section revision	Test in 4th week
MARCH	ECE-4th Sem	Comm. Systems: Pulse Analog modulation, Multiplexing Techniques (2week)	Ppt	Assignment in 3rd week
		Pulse Digital modulation, DPCM, DM. (2week)	Section revision	Test in 4th week.
	ECE-6th Sem	VLSI Design: Sub-system design & layout (2week)	Ppt	Assignment in 3rd week
		NAND-NAND, NOR-NOR, AOI logic. (2week)	Section revision	Test in 4th week
	MTech 2nd Sem	VLSI Design: Design processes, MOS layer, Stick diagram (2week)	Ppt	Assignment in 3rd week
		Basic circuit-concepts - Sheet resistance, type of delays. (2week)	Section revision	Test in 4th week

Signature of the teacher concerned with date

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Department :- E.C.E.

Month	Class	Topic/Chapter Covered	Academic Activity	Test/Assignment
APRIL	ECE-4th Sem	Comm System: Digital Modulation Techniques – ASK, FSK, BPSK, QPSK. (2week)	Ppt	Assignment in 3rd week
		Introduction to Noise – External, internal noise, S/N ratio. (2week)	Section revision	Test in 4th week
	ECE-6th Sem	VLSI Design: Design of combinational elements & Regular array logic. (2week)	Ppt	Assignment in 3rd week
		VHDL programming – Operators, Packages, FSM, Demux (2week)	Section revision	Test in 4th week
	MTech 2nd Sem	VLSI Design: Subsystem, Design and layout (2week)	Ppt	Assignment in 3rd week
		Design examples – design of ALU subsystems. (2week)	Section revision	Test in 4th week

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Name of Institute :- Sat Kabir Institute of Technology and Management, Ladrawan (Jhajjar)
Name of teacher with designation :- SUMIT DALAL, AP.
Department :- ECE

Month	Class	Topic/Chapter Covered	Academic Activity	Test/Assignment
JAN.	ECE 4TH	CS LAB :→ 1. Generation of DSB-SC AM Signal using Balanced Modulator. 2 Generation of SSB - AM Signal 3 To study envelope detector for demodulation of AM Signal.	Practical to be performed	File to be checked
JAN	MTech 2nd Sem	VLSI lab :→ 1. Write a spice programme for CMOS inverter. 2. Write a spice programme for CMOS NAND gate 3. Write a spice programme for CMOS NOR gate.	Practicals to be performed	File to be checked.
FEB	ECE 4th	CS LAB :→ 1. Freq. Modulation using VCO. 2. Detection of FM using PLL & Foster-Seeley method. 3. To study det of PAM / PWM / PPM mod & demodulator.	Practicals to be performed	File to be checked.
FEB	MTech 2nd Sem	VLSI lab :→ 1. Design a D- latch with clk time - period. 2. Design a half-adder using NAND gates 3. Design layout for PMOS in layout editor	Practicals to be performed	File to be checked.
MAR	ECE 4th Sem	CS LAB :→ 1. Generation & Study of Analog TDM four channels 2. Study of ASK, FSK mod. & demodulator. 2. Study of PSK & QPSK mod. & demodulator.	Practicals to be performed	File to be checked.
MAR	MTech 2nd Sem	VLSI lab :→ 1. Design layout for NMOS in layout editor 2. Design layout for CMOS inverter. 3. Design layout for 2-input NAND gate.	Practicals to be performed	File to be checked.
APR.	ECE 4th Sem	CS LAB :→ 1. Study of PCM mod & demodulation 2. Practical problems & viva.	Practical to be performed	File to be checked.
APR.	MTech 2nd Sem	VLSI lab :→ 1. Design layout for 2-input NOR gate 2. Practical problems & viva.	Practical & viva performed	File to be checked.

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